Docket No.: 200205296-1

## **ABSTRACT**

In one embodiment, the present invention is directed to a processor that comprises an instruction pipeline for executing processor instructions wherein the processor instructions define a memory access size and a cache memory for storing cache lines in a plurality of memory banks that have a block size that is greater than the memory access size, the cache memory including mapping logic for storing contiguous groups of bits, of size equal to the memory access size, in different ones of the plurality of memory banks.